1. **Name and Academic Rank:**
   Ali Massoud Haidar, Professor

2. **Education: Degrees, Discipline, Institution and Date:**
   - **Ph.D.** Computer Engineering, Faculty of Engineering, Saitama University, Japan, March 1995
   - **M.E.** Computer Engineering, Faculty of Engineering, Ryukyus University, Japan, March 1992
   - **B.Sc., Electrical Engineering (*Electronics & Communications)*** Engineering, Faculty of Engineering, Beirut Arab University, Lebanon, June 1986

3. **Work experience**
   - **Beirut Arab University:** 1986 ~ 1988, Teaching Assistant, Department of Electrical Engineering, Faculty of Engineering, Beirut, Lebanon.
   - **Hiroshima City University:** April 1995 ~ October 1997, Assistant Professor, Faculty of Information Sciences, Hiroshima, Japan.
   - **Beirut Arab University:** Faculty of Engineering
     1997 ~ 2003, Department of Electrical Engineering
     2003 ~ 2013, Department of Computer Engineering and Informatics
     2013 ~ ……, Department of Electrical and Computer Engineering
   - **European Union:** Feb. 1999 ~ October 2000, expert and counselor to the EU-MEDIS Delegation of the European Commission to the Republic of Lebanon.
   - **Central Bank of Lebanon:** January 1999 ~ January 2000, expert and Counselor for communications, telecommunication, and computer networking.

4. **Service activities**
   - **Order of Engineers** in Beirut
   - **IEEE** (Institute of Electrical and Electronic Engineering)
   - **IEICE** (Institute of Electrical, Information, and Communication Engineering)
   - **Far-East coordinator of the second LAAS**, International conference on Computer Simulation **(ICCS'97)**, American University of Beirut, Lebanon.
   - **Neural networks** group
   - **Petri nets** group
   - **European Society (CST)**
   - **Who's Who in the World:** 1996, Dr. Haidar was on the list of Who's Who in the World guidebook.
   - IEEE/The 2d International Conference on Computers & Applications, Technical Program Committee Member, September 2017, DUBAI, UAE.

5. **Research Interests**
   - Computer Organization and/or Architectures new development
   - Digitalization Systems
   - Neural Networks
   - Multiple-Valued Logic (Theory and Applications)
   - New Trends in Computer Engineering

6. **Principal publications and presentations**:

9.1 Journal Publications

1. Ali Daher, Ziad Osman and Ali HAIDAR "Differential AGC with Offset Stability and Wide Range Frequency Synthesis", Springer Journals, Analog Integrated Circuits and Signal Processing, Manuscript Number : ALOG-D-17-00458, Accepted to be published.

2. Nayif Saleh, Abdallah Kassem and Ali HAIDAR "Energy-Efficient Architecture for Wireless Sensor Networks in Healthcare Applications", IEEE Access, Volume: 6, Issue:1, Page(s): 6478-6486, ISSN: 2169-3536, Digital Object Identifier: 10.1109/ACCESS.2018.2789918, 05 January 2018.
3. Nadine Kashmar, Mirna Atieh and Ali HAIDAR "Identifying the Effective Parameters for Vertical Handover in Cellular Networks Using Data Mining Techniques", Procedia Computer Science on Emerging Ubiquitous Systems and Pervasive Networks (EUSPN-2016), September 2016, London, UK.
4. N., Saleh,, **A. M., Haidar**, W., Itani and H. Shirahama "NNSRAM-Clustering Based Energy Efficient System for Wireless Sensor Networks", International Journal of Enhanced Research in Science, Technology & Engineering, ISSN: 2319-7463, Vol. 4 Issue 12, December-2015.
5. N., Saleh,, W., Itani, A. M., Haidar and H. Nassar "A Novel Scheme to Reduce the Energy Consumption of Wireless Sensor Networks", International Journal of Enhanced Research in Science, Technology & Engineering, ISSN: 2319-7463, Vol. 4, Issue 5, pp: (190-195), May-2015.
6. Robert Chebli, Md. Hasanuzzaman, **Ali Haidar**, Mohamad Sawan "Successive-divider-line ADC dedicated to low-power medical devices", Elsevier, Microelectronics Journal, Vol. 43, pp: 670-679, April 2012.
7. Ali Alaeldine, Richard Perdriau, and **Ali Haidar**, "A Comprehensive Simulation Model for Immunity Prediction in Integrated Circuits with Respect to Substrate Injection", Elsevier, Microelectronics Journal, Vol. 40, No. 12, pp: 1788-1795, December 2009.
8. Oseily, H., **Haidar, A**., and Ahmad, M. "MVL Multiplier Logo Neural Networks Based on Mixed Radices", Alexandria Engineering Journal, Vol. 48, No. 4, pp: 427 – 434, 2009.
9. Kassem, A., Sawan, M., Hamad, M., and **Haidar, A.** "Toward A Miniaturized Generation Of Ultrasonic-Based Devices", Journal of Circuits, Systems, and Computers, World Scientific Publishing Company, Vol. 16, Issue 6, pp. 1027 – 1044, December 2007.
10. Kassem, A., Sawan, M., Boukadoum, M., and **Haidar**, A. "Perception SOC Based on an Ultrasonic Array of Sensors: Efficient DSP Core Implementation and Subsequent", EURASIP Journal on Applied Signal Processing, Volume: 2005, Number: 7, Date: 11 May 2005, pp: 1071 –1081.
11. Shirahama, H., Nasu, K., **Haidar,** A. M., and Fukushima, K., "On-Off Intermittency Observed in a Mutually Coupled Phase-Locked Loops System", **IEE** Proceeding-Science, Measurement, and Technology, Vo. 146, No. 4, July 1999.
12. **Haidar,** A. M. and M. Morisue "Logic Synthesis and Optimization Algorithm of Multiple-Valued Logic Functions", **IEICE** Trans. on Information and Systems, Vol. E77-D, No. 10, pp. 1106-1117, August 1994.
13. **Haidar,** A. M. and M. Morisue "Optimization of Multiple-Valued Logic Functions Based on Petri Nets", **IEICE** Trans. on Information and Systems, Vol. E77-A, No. 10, pp. 1607-1616, October 1994.
14. **Haidar,** A. M., Li, F. Q., and M. Morisue, "Design of Josephson Ternary Delta Gate (δ-gate)", **IEICE** (Institute of Electrical, Information, and Communication Engineering) Trans. on Information and Systems, Vol. E76-D, No. 8, pp. 853-862, August 1993.

15. **Haidar,** A. M., Yamashiro, T., Zukeran, T., and C. Afuso "Design of a Quaternary δ-gate and its Characteristics", Spring Conference, IEICE, 1991, Japan.

9.2 Conference Proceedings

1. Ali Daher, Ziad Osman and Ali HAIDAR "AGC With Signal Offset and Peak-to-Peak Amplitude Stabilization Through Feedback Control", IEEE SENSET-2017, International Conference on Sensors, Networks, Smart, and Emerging Technologies, 12-14 September 2017, Beirut, Lebanon.
2. Iman Haidar and Ali HAIDAR "Axes-Based Key Cryptography", the Third IEEE International Conference on Electrical and Electronic Engineering, Telecommunication Engineering, and Mechatronics (IEEE-EEETEM 2017), 26 – 28 April 2017, Beirut, Lebanon.
3. Ziyad Doughan, Wassim Itani and Ali HAIDAR "'Bio-mimetic Approach in Digital Artificial Neuro-Science", the 3rd IEEE International Conference on Advances in Computational Tools for Engineering Applications (ACTEA), 13 - 15 July 2016, Beirut, Lebanon.
4. **Haidar**, A. M., Saleh, N., W., Itani and H. Shirahama "Toward a Neural Network Computing: A Novel NN-SRAM", NOLTA (International Symposium on Nonlinear Theory and its Applications), 1 - 4 December 2015, Hong Kong, China.
5. Oseily, H. and **Haidar**, A. M. "Hexadecimal to Binary Conversion Using Multi-Input Floating Gate Complementary Metal Oxide Semiconductors", The proceeding of International Conference on Applied Research in Computer Science and Engineering. IEEE-ICAR 2015, Beirut, 8 – 9 October 2015.
6. Hiba BAZZI, Ali **HAIDAR**, Ahmad BELAL "Classification of Routing Protocols in Wireless Sensor Network", International Conference on Computer Applications and Aided Diagnosis, ICCAAD'2015, 18-19 January 2015, Sousse, Tunisia.
7. Rami EL-HAJJ, Mahmoud SKAFI, Ali M. **HAIDAR** "Predicting Global Solar Radiation Using Recurrent Neural Networks and Climatological Parameters", International Conference on Neural Networks, Barcelona (ICNN 2014), February, 27-28, 2014, Spain.
8. L. Mahmoudi, A. Al Azawi, A. Zaart, and A. **Haidar** "A Novel Petri net Model for Image Segmentation Entropic Thresholding based methods", ACTEA12, Dec. 12-15, 2012, NDU, Zouk, Lebanon.
9. Oseily, H. and **Haidar**, A. M. "Multiplier Free and Memory Less RNS to Weighted Converter for the Septenary Moduli Set {7n – 2, 7n – 1, 7n}", Submitted to the NOLTA (International Symposium on Nonlinear Theory and its Applications), October 23rd to 26th, 2012, Palma, Majorca, Spain.
10. A. **Haidar**, K. Fukushima, H. Benner and H. Shirahama "Novel Synchronization Phenomena Observed in a Mutually Coupled Delay Rössler System", proceeding of the ITC-CSCC (The International Technical Conference on Circuit, Systems, Computers and Communications), July 15th to July 18th, 2012, Sapporo, Japan.
11. N. Saleh, A. **Haidar**, A. Kassem and L. Nimri "Neuro-SRAM Technology", proceeding of the NEWCAS (IEEE 10th International New Circuits and Systems Conference), June 17th to 20th, 2012, Montréal, Québec, Canada.
12. Oseily, H. and **Haidar**, A. M. "Octal to Binary Conversion Using Multi-Input Floating Gate CMOS", Proceeding of the 10-th International Symposium on Signals, Circuits and Systems. ISSCS 2011, Iasi, Romania, June 30 – July 1, 2011.

13. Oseily, H. and **Haidar**, A. M. "Residue to Weighted Converter for the Quinary Moduli Set {5n – 2, 5n – 1, 5n}", proceeding of the international conference, NOLTA´2010, Krakow, Poland.
14. Oseily, H. and **Haidar, A. M**. "Quinary Adder LOGO Neural Network Based on Mixed Radices", proceeding of the international conference, NOLTA´2009, Sapporo, Japan.
15. **Haidar, A.**, N. El Ahdab, H. Shirahama, A. Alaeldine "Multiple-Valued Logic Neuron Clock Transformers", Proceeding of the ITC-CSCC´08 (The International Technical Conference on Circuit, Systems, Computers and Communications), Shimonoseki, Japan, July 2008.
16. **Haidar, A.**, M. Jad Hamdan, M. Backer Rashid, H. A. Hamieh, A.A. Issa "A Novel Neural Network Ternary Arithmetic Logic Unit", Proceeding of the ITC-CSCC´08 (The International Technical Conference on Circuit, Systems, Computers and Communications), Shimonoseki, Japan, July 2008.
17. A. Alaeldine, R. Perdriau, M. Ramdani, E. Sicard, M. Drissi, **A. M. Haidar** "Modeling of the Substrate Coupling Path for Direct Power Injection in Integrated Circuits", 2008 IEEE International Symmposium on Electromagnetic Compatibility, Detroit, USA.
18. Oseily, H. and Haidar, A. M. "RSA Encryption/Decryption Using Repeated Modulus Methods", Proceeding of the NOLTA´2008, pp. 712-715, Budapest, Hungary, July 2008.
19. Oseily, H.A., and **Haidar,** A. M., "Arithmetic Algorithms and Circuits to Convert MVL to MVL Coded Decimal and Vice Versa". published in the Proceeding of the IEEE-ICTTA-08 (The IEEE International Conference on Information and Communications Technologies: From Theory to Applications), Damascus, Syria, April 2008.
20. Oseily, H.A., **Haidar,** A. M., and Kassem, A. "Implementation of RSA Encryption Using Identical Modulus Algorithm". published in the Proceeding of the IEEE-ICTTA-08, Damascus, Syria, April 2008.
21. **Haidar,** A. M., Al-Rifai, F., Alaeldin, A. and Bernard, M. F. "A Novel Ternary Controller Unit". published in the Proceeding of the IEEE-ICTTA-08, Damascus, Syria, 7 -11 April 2008.
22. Ahdab, N. and **Haidar,** A. M., Ghabboura, S. "Novel Neural MVL Clock Transformers", proceeding of the CTTACS'07 Conference on Current Trends in the Theory and Applications of Computer Science, Notre Dame University (NDU), Feb. 28-29, 2008, Lebanon.
23. **Haidar,** A. M., "A Novel Logic Oriented Artificial Neural Network to Implement Sequential Logic Circuits", Proceeding of the NOLTA´2006, Bologna, Italy, September 2006.
24. **Haidar,** A. M., Oseily, H. Nassar, E., and Shirahama, H. "Quinary Multiplier LOGO Neural Networks Based on Mixed Radices", Proceeding of the NOLTA´2006, Bologna, Italy, September 2006.
25. **Haidar,** A. M., Ghabboura, S. and Ahdab, N. "A Novel Multi-Valued Logic QAM", Proceeding of the IEEE-ICTTA-06 (The IEEE International Conference on Information and Communications Technologies: From Theory to Applications), Damascus, Syria, April 2006.
26. **Haidar,** A. M., Dernaika, R. and Shibani, F. "A Novel Ternary Quadrature Amplitude Modulation", Proceeding of the IEEE-ICTTA-06 (The IEEE International Conference

on Information and Communications Technologies: From Theory to Applications), Damascus, Syria, April 2006.

27. **Haidar,** A. M., Oseily, H. Nassar, E., and Shirahama, H. "Quirnary Coded Decimal Conversion Techniques", Proceeding of the NOLTA´2005, Bruges, Belgium, October 2005.
28. **Haidar,** A. M., Abu Hoda, A. S., Hamad, M., and Shirahama, H. "LOGO Overcome Combinational Logic Limitations" 18th IEEE Annual Canadian Conference on Electrical and Computer Engineering (CCECE-05), pp. 1061-1064, Saskatoon, Canada, May 2005.
29. **Haidar,** A. M., El-Musawe, A., Haraty, R., Shirahama, H., and Sakamoto, M., "Ternary and Quaternary Decision Diagrams", Proceeding of the CSITeA-04 (The International Conference on Computer Sciences, Software Engineering, Information Technology, E-Business and Applications), Cairo, Egypt, December 2004.
30. **Haidar,** A. M., Shirahama, H., and Magdy, A., "A Novel Neural Network Adder for Prime Numbers", Proceeding of the ITC-CSCC´04 (The International Technical Conference on Circuit, Systems, Computers and Communications), pp. 8D2L-2, Matsushima, Japan, July 2004.
31. **Haidar,** A. M. "A Novel Neural Network Half Adder", Proceeding of the IEEE-ICTTA (The IEEE International Conference on Information and Communications Technologies: From Theory to Applications), p. 0-7803-8482-2/04/$20.00 ©2004 IEEE, Damascus, Syria, April 2004.
32. **Haidar,** A. M., Othman, Z., and Morisue, M. "A New Josephson d-gate for Ternary-Valued Logic" Proceeding of the 14th IEEE International Conference on Microelectronics (ICM), pp. 251-255, Beirut, Lebanon, December 2002.
33. **علي مسعود حيدر: ـ الحوسبة العصبونية: تصميم وتطبيق؛ مجلة أبحاث الحاسوب (مجلة علمية عربية محكمة تصدرها الأمانة العامة لاتحاد مجالس البحث العلمي العربية)، المجلد الخامس، العدد الأول 2001،ص ص 83-92.**
34. **Haidar,** A. M. "A Novel Intelligent Neural Networks for Error Correction Codes", Proceeding of the **NOLTA´2000**, pp. 71-74, Vol. 1, September 17-21, 2000, Dresden, Germany.
35. **Haidar,** A. M., "Neuron-Computing "Design and Applications"", Proceeding of International Conference on Computational Aspects and their Applications in Electrical Engineering (CATAEE'99), 19-20 October 1999, Philadelphia University, Jordan.
36. Fath, A. A., Nakao, Z., **Haidar,** A. M., and Yen-Wei, C. "A Co-evolutionary Algorithm for Multi-Criterion Optimization", Proceeding of **(ISAS/SCI'99)** 3rd World Multiconference on Systemics and, Cybernetics and Informatics & 5th International Conference on Information Systems Analysis and Synthesis, pp. 109-116, July 31-August 4, 1999, Orlando, USA.
37. **Haidar,** A. M., "Optimization of Modulo-R Logic Functions", Proceeding of the International Conference on Scientific Computation **(ICSC-99)**, pp.229-237, Beirut, Lebanon, March 1999.
38. **Haidar,** A. M. and M. Morisue, "Multiple-Valued Logic Oriented Neural Networks", Proceeding of the International **ICSC/IFAC** Symposium on Neural Computing **(NC´98)**, pp. 979-982, Vienna, Austria, September 1998.

39. **Haidar,** A. M. and M. Morisue, "Logic Oriented Neural Networks and its Computer Applications", Proceeding of the **NOLTA´98**, pp. 1169-1172, Vol. 2, Crans Montana, Switzerland, September 1998.
40. Shirahama, H., Koichiro, N., Haidar, A. M. and K. Fukushima, "A Study on Spatial Properties of a Coupled PLL Lattice System", Proceeding of the NOLTA´98, pp. 831-834, Crans Montana, Switzerland, September 1998.
41. **Haidar,** A. M. "A Lebanese Student who created his own fate", La Revue De L'ETUDIANT, August 1998.
42. **Haidar,** A. M. and M. Morisue, **ICSC´97,** Beirut, Lebanon, September 1997.
43. **Haidar,** A. M. and M. Morisue, **PEMC'96** *(International Power Electronics & Motion Control Conference)* Budapest, Hungary, September 1996.
44. **Haidar,** A. M. and M. Morisue, "A Novel Petri Net for Ternary Logic System", Proceeding of the **ITC-CSCC´96** *(International Technical Conference on Circuit, Systems, Computers and Communications)*, pp. 709-712, Seoul, Korea, July 1996.
45. **Haidar,** A. M. and M. Morisue, "A Novel Feedforward Artificial Neural Network to Implement Ternary Logic Systems", Proceeding of the **NOLTA´95**, Vol. 2, pp. 1037-1040, Las Vegas, USA, December 1995.
46. **Haidar,** A. M., and M. Morisue, "Petri Nets for Ternary Logic System", Proceeding of the **JTC-CSCC´95**, pp. 754-757, Kumamoto, Japan, July 1995.
47. **Haidar,** A. M. and M. Morisue, "A Novel MVL Artificial Neural Network", Proceeding of the **MVL-95 Technical Conference**, Vol. MVL-95, No. 1, pp. 73-79, Japan 1995.
48. **Haidar,** A. M. and M. Morisue, "A Novel MVL Artificial Neural Network", Technical Report of Multiple-Valued Logic Meeting, January 20, 1995, Japan.
49. **Haidar,** A. M., and M. Morisue, "Synthesis of Multiple-Valued Logic Functions Based on Petri Nets", Proceeding of the **7th Franco-Japanese** on Combinatorics, Optimization and Computational Geometry, Tokyo, Japan, June 1994.
50. **Haidar,** A. M., and M. Morisue, "Ternary Logic Oriented Neural Networks", Proceeding of the **3rd IIZUKA´94** *(3rd International Conference on Fuzzy Logic, Neural Nets and Soft Computing)*, pp. 59-62, Iizuka, Japan, August 1994.
51. **Haidar,** A. M., and M. Morisue, "ペトリネットに基づく多値論理関数の合成 Multiple-Valued Logic Synthesis Based on Petri Nets", Technical Report, IEICE, CST94-8, pp 55 – 62, Tokyo, April 1994.
52. **Haidar,** A. M., Morisue, M. and S. Watanabe, "Logic Oriented Neural Networks", Proceeding of the **NOLTA´93** *(International Symposium on Nonlinear Theory and its Applications)*, Vol. 2, pp. 589-592, Hawaii, USA, December 1993.
53. **Haidar,** A. M., and M. Morisue, "Optimization of Multiple-Valued Logic Functions", Proceeding of the **ECCTD´93:** *(European Conference on Circuit Theory and Device)*, pp. 1081-1086, Davos, Switzerland, September 1993.
54. **Haidar,** A. M., and M. Morisue, "Multiple-Valued Logic Neural Networks", Proceeding of the **JTC-CSCC´93**, pp. 813-817, Vol. 2, Nara, Japan, July 1993.
55. **Haidar,** A. M., and M. Morisue, "Petri Nets over Multiple-Valued Logic Systems", Proceeding of the **JTC-CSCC´93** *(Joint Technical Conference on Circuit, Systems, Computers and Communications)*, pp. 336-341, Vol. 1, Nara, Japan, July 1993.
56. **Haidar,** A. M., C. Zukeran, and C. Afuso "Synthesis of Multiple-Valued Logic Networks Based on Delta-gates", MVL Conference in Japan, Vol. 14, No. 5, pp. 5:1-5:10, July 1991, Saitama, Japan.

57. **Haidar,** A. M., and C. Zukeran, "Design of a Quaternary Delta-gate and It's Characteristics", **IEICE** (Institute of Electrical, Information, and Communication Engineering) conference, Shikoku, Japan, 1990.